SENS-TECH
SENSOR TECHNOLOGIES

XDAS-V2
X-ray data acquisition system

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user manual

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XDAS-V2 X-ray data acquisition system

contents

1 introduction

1.1 general

XDAS is a modular system of boards for use in any X-ray linescan application. Each board has 64 or 128 channels, corresponding to a detector pitch of 2.5, 1.6, 0.8 or 0.4 mm. Multiple boards can be connected in series and detectors can be butted end-to-end to provide a continuous array.

Data output is in 16 bit format. The system can be interfaced to a PC via:

- USB2 Local (5m maximum)
- USB2 Remote
- PCI-7300A data I/O card
- standard frame grabber card

Control signals are transmitted to the board via the USB2 connection or an RS485 serial interface, which can be easily generated from a standard RS232 serial port, using an RS232 to RS485 converter.

X-rays are detected using a scintillator and a photodiode array. Scintillators, such as phosphor strip, CsI(Tl), or $CDW0_4$ are offered to cover a wide energy range from 30 keV to 450 keV.

1.2 applications

These include security, food inspection, thickness measurement, bone densitometry and non-destructive testing.

1.3 features

- 2.5, 1.6, 0.8 or 0.4 mm detector pitch
- range of scintillator types available
- up to 21504 (128x24DHx7SP) channels in a system
- simultaneous data acquisition and read-out
- dual energy option
- wide dynamic range
- 16 bit output
- high speed USB2 or parallel RS485 link to CPU

1.4 product

hardware

A standard XDAS board is supplied in 2 basic formats, depending on whether a dual energy version or a single energy version is required.

- The dual energy version has 64 detector channels on each side of the board for detection of low and high energy X-rays.

- The single energy version has 64 or 128 detector channels on one side of the board only.

XDAS-V2 is a series of products that consists of two basic building blocks:

- A detector head (**DH**) board populated with custom radiation detectors. It is possible to daisy chain up to12 DH boards.

- A signal processing (**SP**) board that allows the user to control the operation of two chains of 12 DH boards each. It is also possible to connect up to 7 SP boards together to form a single system output.

Further details can be found in the XDAS-V2 datasheet available from the Sens-Tech website: www.sens-tech.com.

XDAS units should be operated within a housing to provide electrical and radiation screening. A test box can be supplied for system evaluation.

Connection cables for module interconnection and for connection to a PC can be supplied as required. They include the communications link and power connections. Signal terminators must be used for the local and system buses and must be fitted to the master signal processing board and the last detector board of every sub chain of an XDAS system. These can be supplied to order.

standard software

Standard XDAS software is supplied to permit basic operation and evaluation of the system. The software enables the user to set signal integration time and sub-sample rate, acquire and log data, and perform offset and gain corrections on live data. This is described in **section 4, start up software.**

user software applications

Users may wish to write their own independent software application to provide system control and data acquisition. This is described in **section 5 advanced, user guide.** A Software Development Kit (SDK) is available. This provides the data acquisition source code.

module and system operation

This is described in **section 7, module system and operation.**

2 precautions

2.1 supply voltage

Ensure the +6V supply voltage does not exceed +9V or fall below +5.5V. Exceeding these limits may result in unpredictable behaviour. The power supply must not exceed the absolute maximum ratings which can cause permanent damage to the unit. (**see appendix A**).

2.2 maintenance

There are no user maintainable components. The user must not attempt disassembly. Boards must be returned to **Sens-Tech** for service or repair.

2.3 cleaning

The Boards may be hand cleaned using conventional printed circuit board techniques. Residues should not be left on the board that could affect the performance of the sensitive front-end analogue electronics.

2.4 environment

The Boards must not be exposed to levels outside those specified in **appendix B**.

2.5 radiation

The Boards use components of limited radiation hardness. Additional shielding is required to protect the electronics from the X-ray source.

2.6 connections

Always make connections to the Boards with the power supplies switched off.

2.7 electrical screens

The complete system of XDAS boards must reside in a fully shielded enclosure, to protect from external noise and interference.

3 installation

The following instructions will enable users to operate the XDAS unit using the software provided. Results can be taken immediately and the hardware setup can be checked for correct operation.

3.1 system requirements

Intel Pentium® III or faster CPU
(A USB2.0 capable PC is required for USB2 interface)
Microsoft Windows® 98, 2000 or XP
A mouse or a tablet
VGA or higher resolution monitor
CD drive

+6V low noise DC power supply

3.2 interfaces (see appendix A for details)

The diagrams of **appendix D** show three different types of connection: USB2, PCI-7300A and a frame grabber card connection. Please make connections as shown.

3.2.1 control interface

Set up the serial interface as follows:

type	RS485
baud rate	9600
data bits	8
parity	odd
stop bits	1

USB2 connection does not require a separate serial interface.

3.2.2 data interface

One of three types of interface can be used: USB2; PCI-7300A Data I/O card or frame grabber. These should be set up as follows:

USB2

type	USB 2.0
data rate	2.5-20 Mbytes per second sustained
mode	Bulk transfer mode.
Buffer	130kBytes of cache buffer

A standard USB B socket is used, conforming to industry standards.

PCI data I/O card

type	TTL, parallel 8 bit
data rate	2.5-20 Mbytes per second clocked using gated PCLK
mode	synchronous

Signal types and connector definition are detailed in **appendix A.**
Details of the synchronous protocol are defined in **appendix F**.

Frame Grabber

type	RS422, parallel 8 bit
data rate	5-20 Mbytes per second clocked using PCLK
mode	synchronous

Signal types and connector definition are detailed in **appendix A.**
Details of the synchronous protocol and line and frame synchronization are defined in **appendix F**.

3.2.3 detector interface

Where users are fitting their own detectors, details of the detector connections, for 16 and 32 channel detectors, can be found in **appendix G**.

3.2.4 ID address

Ensure dip switches are set on each signal processing module, based on the position of each module in the system chain. For systems with only one processing board, the address is always set to address 1.

address	address positions (jumper or dip switch)		
	2	1	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Note that each board is factory set to address '000'. The user must set the address for each SP board in the system before use.

Address '001' is Master.

3.2.4 Board Header

Set the dip switch H to ON position. This enables the addition of two header bytes in the beginning of each data block identifying each detector board. This setting is required for XDAS software and is optional for customer specific software.

3.3 mounting (see mechanical interface drawing appendix H)

Four mounting holes, suitable for M3 fasteners are provided on each detector module to allow the securing of the modules into the system. The signal processing module has eight mounting holes suitable for M3 fasteners. Each provides a ground connection for the board.

Care must be taken to ensure the modules are electrically screened from external interference. They must also be screened from the X-ray beam using appropriate techniques.

3.4 software installation

Insert the **XDAS** software CD into the computer's CD-ROM drive.
If the setup program does not auto-run, carry out the following.

- Select **Run** from the **Start** menu.
- In the command line box, type **d:\setup** (where d is the letter of your CD-ROM drive), then click **OK** or press the **Return (↵)** key.
- Follow the on screen instructions.
- The setup program creates a program icon in the **Start** menu.
- Browse and click the XDAS Demo (V1x/V2) icon to start the program.

3.5 software operation (version 3.41) – V1x/V2

On entering the program, the driver selection window is displayed first. Select the correct option applicable to the type of data interface you are using and click **OK**. The software will then display the **Command Interpreter** box and the **Data Acquisition** window.

The system is now ready to be used. Data acquisition parameters are set up on the **Command Interpreter** and sent to XDAS using the **Send** button. The button turns green after a successful XDAS configuration.

The system will commence data acquisition by pressing the **Start** button. Detailed setting-up instructions can be found in **section 4, start up software**.

4 start-up software

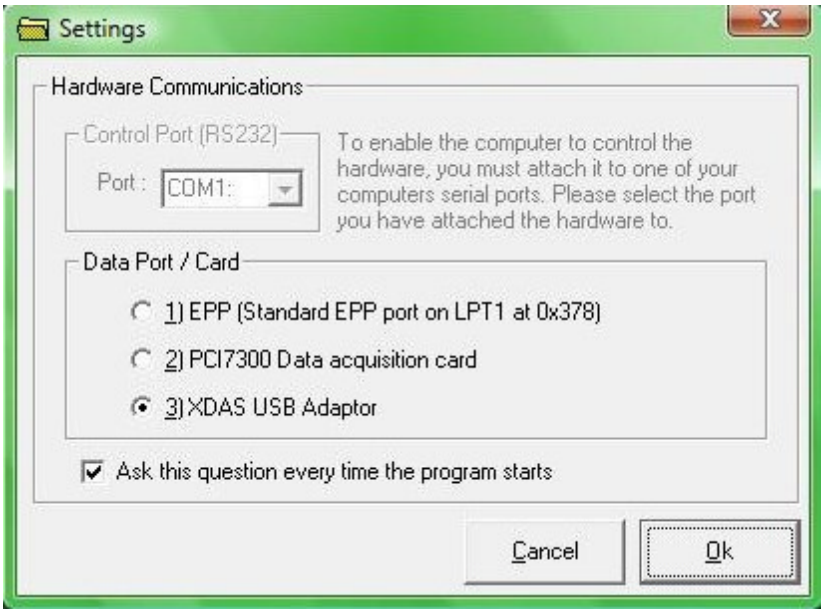
XDAS Software is provided with the unit to allow immediate use of the product. Custom user programs may be required and **section 5, advanced user guide** defines the necessary interface protocol for users to follow.

These instructions are written for Microsoft Windows XP™. The software provided with the unit can be operated by carrying out the following steps.

Before using the software the module(s) must be connected together and to the host PC as stated in **section 3, installation.**

A copy of the latest version of XDAS Demo software must be installed.

Start the XDAS demonstration software by browsing to Start\All Programs\XDAS\XDAS Demo (V1x). Select the applicable cable interface option in the driver selection window and click **OK**.

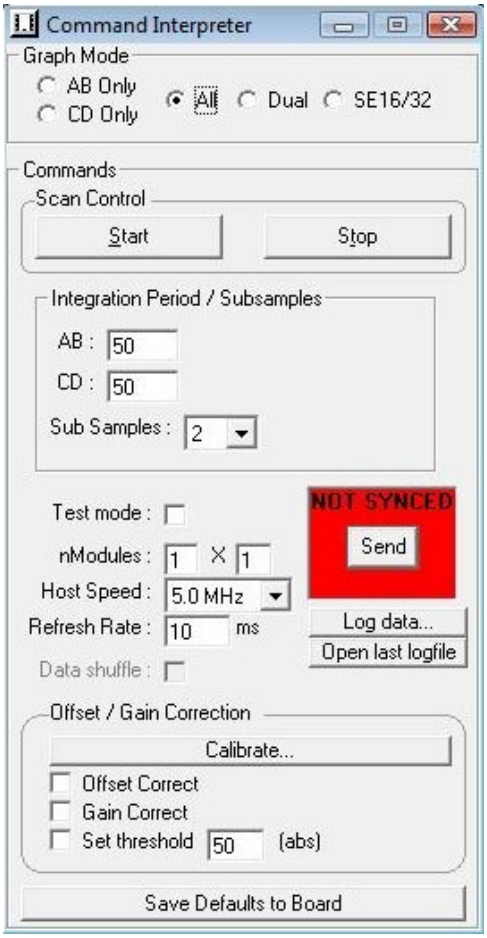


**The EPP mode is not available on XDAS-V2.*

4.1 command interpreter

In the **Command Interpreter** set up the following default configuration:

Graph mode	:	All
Integration period AB	:	50 (i.e., 500us)
Integration period CD	:	50 (i.e., 500us)
Subsamples	:	2
Test mode	:	unchecked
nModules	:	1 x 1
Host speed	:	5MHz
Refresh rate	:	10ms



Now click on the **Send** button which should turn **Green** indicating successful XDAS setup.

4.1.1 graph mode

The axis of the graph is automatically scaled to correspond to the total number of channels depending on the number of modules in the system. The following modes can be set via the **Command Interpreter**:

AB This selects only channels 1 to 64 to be displayed from each module.
CD This selects only channels 65 to 128 to be displayed from each module.
ALL This selects all channels to be displayed in a single line.
Dual This selects modes AB and CD to be displayed at the same time, as different colours on the same x and y axis.

4.1.2 scan control

This starts or stops the data acquisition process based on the last set of settings sent from the **Command Interpreter**.

4.1.3 integration period

This allows the user to set either identical or different integration periods for channels 1 to 64 and 65 to 128 on each module. The integration period and can be set between 1 and 50000 (10 µs to 0.5 s) in steps of 10us.

4.1.4 test mode

This mode must only be used with the integration time set to a maximum of 30us for 2pF mode and 150us for 10pF mode.

The test mode injects a factory defined signal into the odd and even inputs such that the odd numbered channels produce an output twice to that of even numbered channels. This feature allows the testing of the system in the absence of an external signal.

4.1.5 sub-sample

There is a choice of three different levels of sub-samples: 1, 2, and 4.
When **Sub-samples** is activated, multiple integration periods are taken dependent on the number of sub-samples requested. This allows the dynamic range of the module to be extended. The user may perform further sub-sampling in software.

4.1.6 modules

This input tells both the hardware and the software how many modules are connected in the system.

A	X	B	= Analogue x Digital

4.1.7 refresh rate

This sets the software refresh rate for acquiring new data and can be varied from 1 ms to 100 s.

4.1.8 data log

When data logging is activated a separate menu is displayed requesting the file name, number of data points required, and whether to add calibration data and command interpreter settings. The system then logs data based on these parameters and saves it in csv format.

4.1.9 open last log file

This allows the last set of data to be logged or to be reloaded for analysis or viewing.

4.1.10 calibrate

The calibration mode allows the user to acquire offset and gain calibration parameters. These are as follows:

offset: takes a reading based on the current settings and stores the figure for each channel as the offset correction factor. This is carried out with no signal present.

gain: takes a reading based on the current settings and calculates the gain correction factor for each channel to give 95 % of full scale. This should be carried out with maximum signal present on all channels.

The calibrate function allows 3 display options as follows:

offset correct: this automatically deducts the stored offset from all readings before displaying and storing.

gain correct: this automatically calibrates with the stored gain correction factor for each channel before displaying and storing.

set threshold: this allows all readings below a set number (0 to 65536) to be set to zero, to allow for threshold detection.

The calibration factors can be applied to either live or static data.

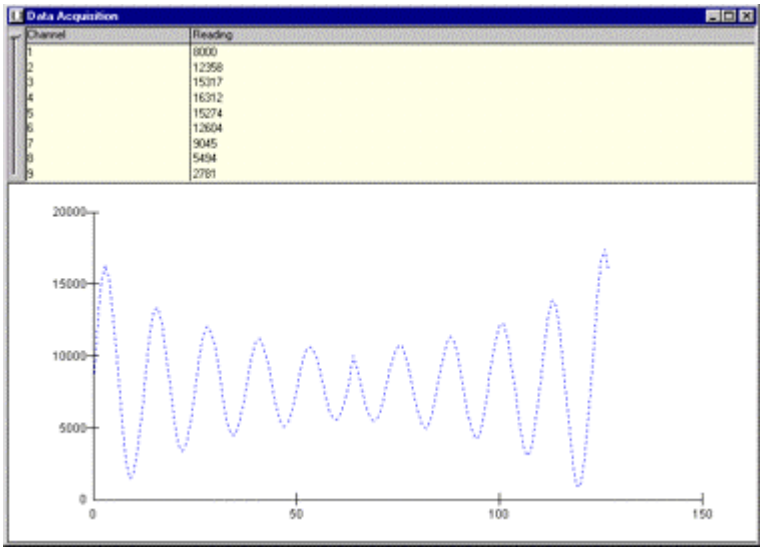
4.1.11 save defaults

This allows the current settings in the **Command Interpreter** to be set as the module power-on defaults that are used on initial switch-on.

4.1.12 send

This transmits the current parameters setup on the **Command Interpreter** screen to the hardware. The **Send** box remains highlighted in Red if settings have been changed and not transmitted to XDAS.

4.2 X-ray data acquisition



The following facilities are available from the **X-ray Data Acquisition** menu bar:

file

open:	enables the user to select a previous set of results for analysis.
save/save as:	enables the user to save a set of results.
settings:	allows the data and control interface to be selected as defined in **section 3, installation**.
exit:	exits the program.

edit

copy:	copies data to the clipboard to enable it to be pasted into other software applications, such as a spreadsheet or word processor.

view

graph only:	displays graph only.
channel as:	channel/number: table referenced to channel numbers (1 to 8064) or module/channel: table referenced as module and channel number
graph	(ie. 1/63 = module 1 channel 63).
type:	selects bar, line or bar/line combination display types.

window

data acquisition:	switches on/off the graphical display.
command interpreter:	switches on/off the command interpreter.
cascade:	allows data acquisition and command interpreter to be cascaded.

help

help:	future option. For help contact the **Sens-Tech** technical help line.
About:	Opens a software information shield.

5 advanced user guide

XDAS-V2 has two interface channels. These are the **control channel** and the **data channel**. The **control channel** is used to issue commands to the XDAS system whereas the **data channel** is used only to receive channel data from the XDAS system. In this section, hexadecimal numbers are indicated by the prefix 0x.

5.1 the control channel

The **control channel** is used to issue commands to the XDAS system. It is an RS485 serial input and is bussed to all the modules in the system. External connections to this bus are typically made using pins 8 [SCTRL+] and 7 [SCTRL-] of the **system bus** connector.

5.1.1 command format

All commands sent to the XDAS system follow a generic pattern described below.

All commands start with the byte 0xC0. This is followed by one or two byte(s) representing the command (Cmd). Where a command has parameters, these are sent immediately after the Cmd byte.

5.1.2 parameter format

There are two types of parameters that can be sent with a command. These are **one byte** and **two byte** parameters.

one byte parameters are sent simply as one byte.

two byte parameters however, must be split into nibbles (half bytes) and sent as four separate bytes. The most significant byte is sent first.

An example of this is given in **section 5.1.4**.

5.1.3 command listing

The commands for controlling an XDAS system are shown below.

Cmd byte	function	parameter type (see section 5.1.2)	description
0x00	start scan	**none**	start continuous scan
0x01	stop scan	**none**	stop scan default = OFF
0x02	set number of SP boards	**one byte**	sets the number of signal processing boards in the system N = 1 to 7 default = 2
0x03 *	set integration period AB	**two byte**	sets the integration period for block AB (ch1-64). default = 68 (680us)
0x04	set output data bus speed	**one byte**	sets the PCLK frequency where 0=2.5, 1=5, 2=10, 3=20MHz default = 2 (10MHz)
0x05	set sub-samples	**one byte**	sets the sub-samples, S where N is the parameter. $S = 2^N$ default = 0 (1 ss)
0x06	test mode ON	**none**	enable test mode default = OFF
0x07	reserved		
0x08 *	set integration period CD	**two byte**	sets the integration period for block CD (ch65-128). default = 68 (680us)
0x09	reserved		
0x0A	test mode OFF	**none**	disable test mode default = OFF
0x0B	set number of DH boards	**one byte**	sets the number of detector boards in the system. N = 1 to 24 default = 12
0x0C	reserved		
0x0D	save boot defaults	**none**	Saves current settings as power on defaults.
0x0E	reserved		
0x0F	reserved		

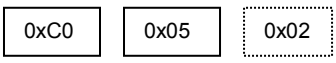
* the integration time, T, is derived from the integration period, P as follows:

$T = 10\ \mu s \times N$

5.1.4 example commands

Set number of sub-samples in system to 4

$4 = 2^2$



Set integration period to 2600 (2600 = 0x0A28) on both AB and CD

0xC0	0x03	0x00	0x0A	0x02	0x08
0xC0	0x07	0x00	0x0A	0x02	0x08

Start Scanning

0xC0	0x00

5.1.5 scan trigger (nSCAN)

There is an option to start and stop the scan using hardware, for example, to synchronise scanning to an X-Ray shutter.

nSCAN is a 5V CMOS signal (locally pulled high) and should be input to the first SP board in the system. The module address does not matter. **nSCAN** is then bussed to other modules over the system bus.

By default, **nSCAN** is a level triggered pin and as such, when **nSCAN** is Logic 0, continuous scanning begins. When **nSCAN** is Logic 1, continuous scanning stops.

Switch A switches **nSCAN** from **level triggering** to **edge triggering** on both rising and falling edges.	Set nSCAN edge triggered	Not Set nSCAN level triggered **(factory setting)**

For edge triggering, there is one line acquisition and readout for each of the rising and falling edges. The integration time and subsamples are set using the serial control interface. XDAS ignores any nSCAN edges that appear while the current integration cycle is in progress.

It is advised to use an opto-coupler to isolate nSCAN from XDAS if the trigger source is referenced to a different ground plane.

5.2 the data channel

The **data channel** is used to receive channel data from an XDAS system. It is an 8-bit wide, RS485 (differential) parallel data bus running through all signal processing modules in the system.

In a multi-processor system, the external connection between the XDAS system is made from the module with the highest address and **not** from the module with address 1. The modules send their data in order of address, starting at address 1.

5.2.1 Dip switches affecting the data transfer protocol

The data transfer protocol is set up using dip switches **B, C**, **F,** and **H.**

switch B allows the user to change the order of channel readout from each detector board.	Set readout reversed	Not set standard output **(factory setting)**
switch C allows the user to change the order of detector board readout from each signal processing board.	Set standard output	Not set readout reversed **(factory setting)**
switch F switches the gated pixel clock (PCLK) mode. When PCLK is gated, PCLK only clocks valid data. When PCLK is un-gated, PCLK clocks continuously. In un-gated mode, LVAL ± is used to validate the data. Un-gated mode is normally used for frame-grabber cards. The un-gated mode is available only in single SP board systems.	Set PCLK ungated	Not set PCLK gated **(factory setting)**
switch H controls the address header prefix. When enabled, two header bytes are prefixed to each packet data per module. The first bytes represents the SP board ID and the second byte represents the DH board ID. This enables software to verify that it is in sync with the data.	Set header prefix enabled **(factory setting)**	Not set header prefix disabled

DIP switches B and C allow to user to set XDAS to one of all the possible combinations of the readout direction.

5.2.2 data format

Data bytes are presented on the data output connector. The data from each module is organised as shown below. The channels are output in order from 1 to 128. Channel data is two bytes wide.

If switch H is set, a two byte header is added to the output of each module. The header contains the address of the signal processing board (m) in the first byte and the module number (n) in the second.

For example, data output for the first DH board connected to first SP board with switch H (two header bytes) and switch E (digital test pattern enable – section 5.3) are set to ON is given below.

SP address*	**DH address***	**CH1 Data**			**CH128 data**	
0x0m	**0x0n**	low byte	high byte	⟶	low byte	high byte
0x01	**0x01**	0x00	0x00		0xFC	0x01

The test mode changes when the readout order is changed using switch B and switch C corresponding to data from different RAM locations. The header bytes remain the same.

5.2.2.1 synchronous mode

Data is output synchronised to PCLK, running at 2.5/5/10/20 MHz. This allow up to 20Mbytes/s data output. Both USB2 and PCI7300 interfaces are able to meet these requirements.

	J1 & J2
37	PCLK -
38	PCLK +

Data must be read from the data pins on the NEGATIVE edge of PCLK.

5.3 additional configuration jumpers

switch D is for factory testing only. This forces the system to boot from hardware defaults and is useful if saved boot data is corrupted.	Not set **(factory setting)**
switch E causes the ADC to be disconnected and replaced by a known incrementing digital test pattern (a ramp function). All data processing is performed on this data in exactly the same way as if it were real ADC data, enabling the digital electronics to be tested.	Set test pattern ON Not set test pattern OFF **(factory setting)**

switch G is used to change the integration capacitance on the front end charge integration amplifiers.	Set 2 pF Not set 10 pF **(factory setting)**

6 troubleshooting

6.1 No response

Check all the connections have been made correctly including data and power cables and termination sockets.

Check the +6 V power supply is on and correctly set.
(Note that the system will not operate if voltage at any module drops below +5.5 V).

Check that module address has been setup correctly using DIP switches.

Check that the unit has been set up properly on the software command window.

6.2 Count overflow or very high count rates

Check module optical connection is light-tight.

Check the front end gain setting on DIP switch G.

6.3 Half full scale output even without any signal

Remove and reinsert the local bus termination socket carefully.

Check that offset adjustment potentiometer VR1 is not damaged.

6.4 Output data/image is scrambled

Check that the readout order is set correctly using DIP switches B and C.

6.5 Output is not synchronised

Check that header bytes are enabled/disabled as required using the DIP switch H.

6.6 Software will not install

Check computer running Microsoft Windows® 98, or later.

6.7 No readings can be taken

Check unit connected to the USB2 port, data I/O card or frame grabber has been correctly installed.

6.8 System not operating correctly with multiple signal processing boards

Check addresses are set correctly.

Please contact Sens-Tech for further support.

7 module and system operation

7.1 XDAS module operation

A schematic of a single XDAS module is shown on the **module block diagram, appendix C**.

The detector array is connected to the board via 4 x 16 way (1.6 mm pitch) or 4 x 32 way (0.8 mm pitch) headers. The dual energy boards are available in 1.6 mm or 2.5 mm pitch, and has a second row of detectors connected to the back of the board. The single energy board will accept 1.6 mm or 0.8 mm pitch arrays.

Current from the photodiodes is measured by a custom designed microcircuit containing 128 charge integrating amplifiers and a multiplexer. The microcircuit provides two serial analogue outputs, corresponding to amplifier output voltages at the beginning and end of signal integration. These are fed via a differential amplifier, eliminating common mode noise, to a 14-bit ADC.

The system can operate in continuous mode with one set of data being read out while the next set is being acquired. In continuous operation the dead time is less than 1 µs.

The maximum charge that can be collected per cycle depends on the choice of the storage capacitors, one per channel, which are internal to the microcircuit. These can be set to 2 pF or 10 pF. High linearity is maintained with a voltage swing of 1.5 V providing charge storage of 3 pC or 15 pC per cycle.

If higher dynamic range is required, a facility for sub-sampling and data summation is incorporated on-board. This is the image data store **(see module block diagram, appendix C)**. Up to 4 sub-samples can be acquired and stored in the image data store, which is a 16 bit device. When data is ready for transmission, the 16 bits are transmitted via the chosen interface to the host CPU.

Operation is controlled by a gate array (FPGA), which provides the central intelligence for the board and the timing and control signals for system operation. The gate array is based on fused link technology, providing a high level of radiation hardness.

User settings to control integration times, sub-sampling, and refresh rate, together with information on system configuration, are transmitted via an RS485 interface and can be stored in non-volatile RAM such that on switch-on, the system is initiated in the last mode saved. The RS485 is compatible with the RS232 serial port on standard PCs using the interface converter supplied as part of the cable set.

The data output bus is a differential RS485 link (multi-drop RS422) capable of transmitting at 2.5/5/10/20 MB/s. Interface to a PC is via USB2, PCI-7300A data I/O card or frame grabber card. The same configuration of XDAS board is used for each mode but a different cable set is required to connect to the PC. If USB2 mode selected, no additional board is required for a PC. USB2 cable is capable of providing a single link for both data and control buses.

7.2 XDAS system operation

Up to 12 detector boards can be daisy-chained to form a single detector system. Each SP board can process two chains of 12 DH boards each. It is further possible to daisy chain up to 7 SP boards. The first SP board in the system acts as the master board, ensuring that all boards in the system are synchronised. The master board transmits the image data from all boards to the host CPU via the RS485 link, see the system block diagram, **appendix C**. It also transmits all control settings from the host to the slave boards.

To enable control settings to be made, each module is set up with a unique address, from 1 to 7. Address 0 is reserved as a broadcast address for all modules. The address is set by means of DIP switches links on the board.

The SP boards share the multi drop system bus. One of either the speed of the communications link or the ADC sample rate is normally the factor limiting data acquisition and read-out rate for the system.

Sens Tech provides an XDAS-V2 system builder tool for rapid system configuration or alternatively, contact Sens-Tech for support and advice.

appendix A

XDAS interface characteristics

absolute maximum ratings

	test conditions	min	typ	max	units
supply voltage (+6 V)		+5.5	+6.0	+9.0	V

DC characteristics (T_a = 25 °C supply = +5.5 V to +6.5 V)

	test conditions	min	typ	max	units
digital (TTL 5 V)					
input low volts (max)	O/P sinking current			0.8	V
input high volts (min)		3.7			V
output low volts (max)				0.2	V
output high volts (min)		4.7			V
+6 V supply (SP)					
supply volts		+5.5	+6.0	+9.0	V
supply current: Master board with termination sockets		200		700	mA
supply current: Each slave board		100		400	mA
+6 V supply (DH)					
supply volts		+5.5	+6.0	+9.0	V
supply current		110	125	140	mA

**XDAS V2 may not operate if the supply voltage drops below +5.25V or exceeds +9.5V.There is limited over voltage protection for up to +13.0V.*

appendix A (continued)

signal processing board

connector J5 - 40 way 2.54mm pitch male IDC header for system bus mates with 40way 2.54mm pitch female IDC connector

pin	designation	description	signal type
1	GND	Ground	-
2	nRST	System Reset	TTL (5V)
3	LA2-	Local address 2	RS485
4	LA2+		
5	NC	Not connected	-
6	NC	Not connected	-
7	SCTRL-	System Control	RS485
8	SCTRL+		
9	nSCAN	Scan Enable	TTL (5V)
10	LAEN+	Local Address Enable	RS485
11	LAEN-		
12	LA0+	Local Address 0	RS485
13	LA0-		
14	LA1+	Local Address 1	RS485
15	LA1-		
16	NC	Not Connected	-
17	NC	Not Connected	-
18	NC	Not Connected	-
19	LVAL-	Line Valid	RS485
20	LVAL+		
21	D7-	Data Bit 7	RS485
22	D7+		
23	D6-	Data Bit 6	RS485
24	D6+		
25	D5-	Data Bit 5	RS485
26	D5+		
27	D4-	Data Bit 4	RS485
28	D4+		
29	D3-	Data Bit 3	RS485
30	D3+		
31	D2-	Data Bit 2	RS485
32	D2+		
33	D1-	Data Bit 1	RS485
34	D1+		
35	D0-	Data Bit 0	RS485
36	D0+		
37	PCLK-	Pixel Clock	RS485
38	PCLK+		
39	MCLK-	Master Clock	RS485
40	MCLK+		

appendix A (continued)

Connectors J1 - 4 way polarised male header MOLEX 2203-5045
J2 - 4 way polarised RA male header MOLEX 2205-7045
mates with crimp housing MOLEX 5037-5043
and crimp MOLEX 870-1040

pin	designation	description	signal type
1	GND	Ground	-
2	nSCAN	Scan Initiation	TTL
3	+6 V	6 V Power	DC
4	+6 V	6 V Power	DC

Connectors J3 & J4 - 50 way 2mm pitch IDC header for local bus E-TEC SLS-050-H562-55/2
mates with 2mm pitch female IDC connector E-TEC IDS-050-S200-95/P

J3 connects to modules 1 to 12 and J4 connects modules 13 to 24. Both sub chains must be terminated.

detector head board

connectors J1 - 4 way polarised male header MOLEX 2203-5045
J2 - 4 way polarised RA male header MOLEX 2205-7045
mates with crimp housing MOLEX 5037-5043
and crimp MOLEX 870-1040

pin	designation	description	signal type
1	GND	Ground	-
2	nSCAN	Scan Initiation	TTL
3	+6 V	6 V Power	DC
4	+6 V	6 V Power	DC

J1 and J2 are optional for a system with less than six detector head boards. In a larger system ,it is acceptable to connect power only to the last DH board in every sub chain.

Connectors J3 - 50 way 2mm pitch male IDC header for local bus output
J4 - 50 way 2mm pitch male IDC header for local bus input
E-TEC SLS-050-H562-55/2
mates with 2mm pitch female IDC connector E-TEC IDS-050-S200-95/P

J3 is the output connector and J4 is the input connector. The output of each DH board is connected to the input of the next to form a chain of up to 12 DH boards. The output of the first DH board is connected to relevant local bus connector on the SP board. Each SP board can accept two daughter chains of 12 DH boards each. The input of the first DH board in every chain must be properly terminated.

appendix B

environmental conditions

1 temperature (operating)

+5 to +35 °C

2 sinusoidal vibration (all 3 axes, non-operating)

10 to 500 Hz for 10 cycles in each axis, at peak amplitude of 2 g,
1 octave/min.

3 random vibration (all 3 axes, non-operating)

10 - 20 Hz roll on	6 dB/octave
20 - 50 Hz	0.02 g^2/Hz
50 - 500 Hz roll off	6 dB/octave
at 500 Hz	0.001 g^2/Hz

4 humidity (non-condensing)

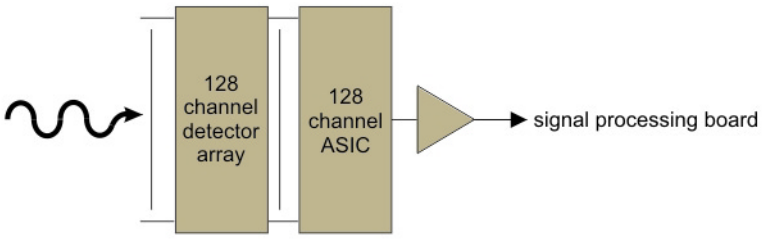
93 % at 30 ºC

5 pressure (for transportation)

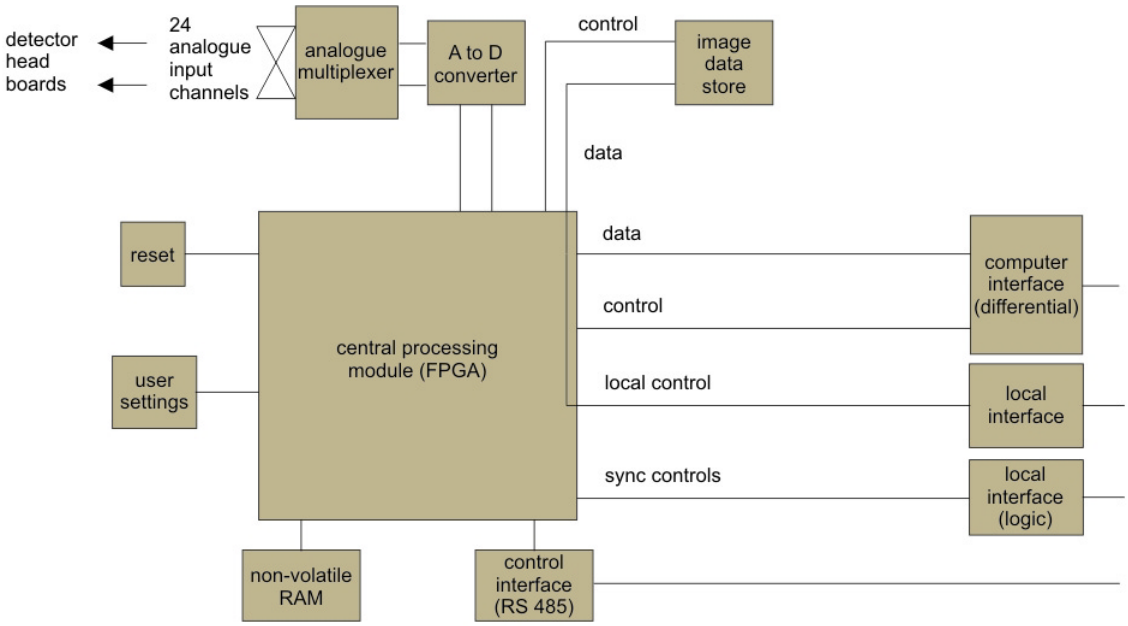
can withstand pressure reductions from 68 kPa (1 bar) to 100 kPa (0.68 bar).

appendix C

detector head board

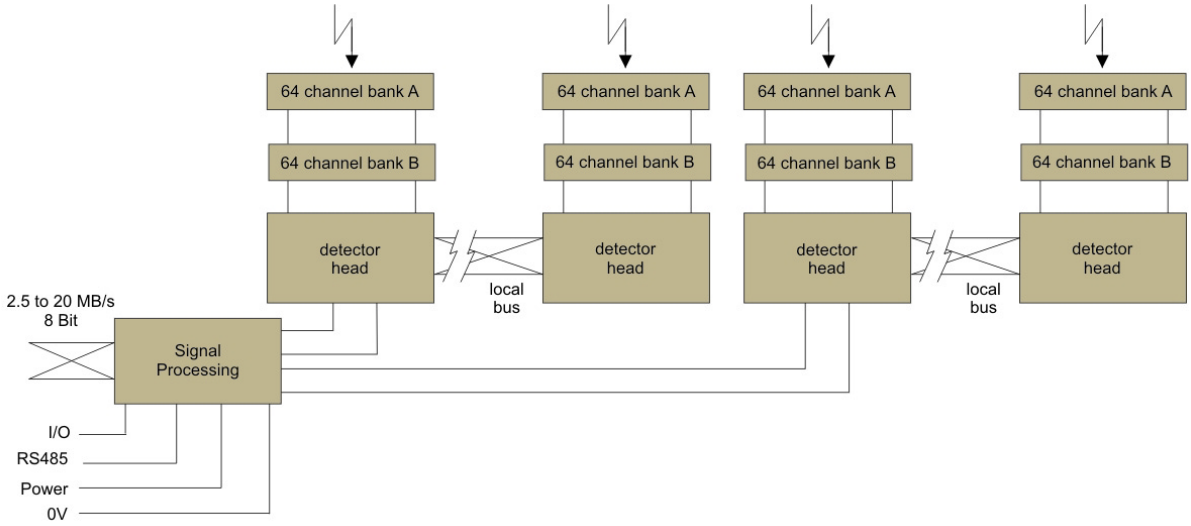


signal processing board



appendix C (continued)

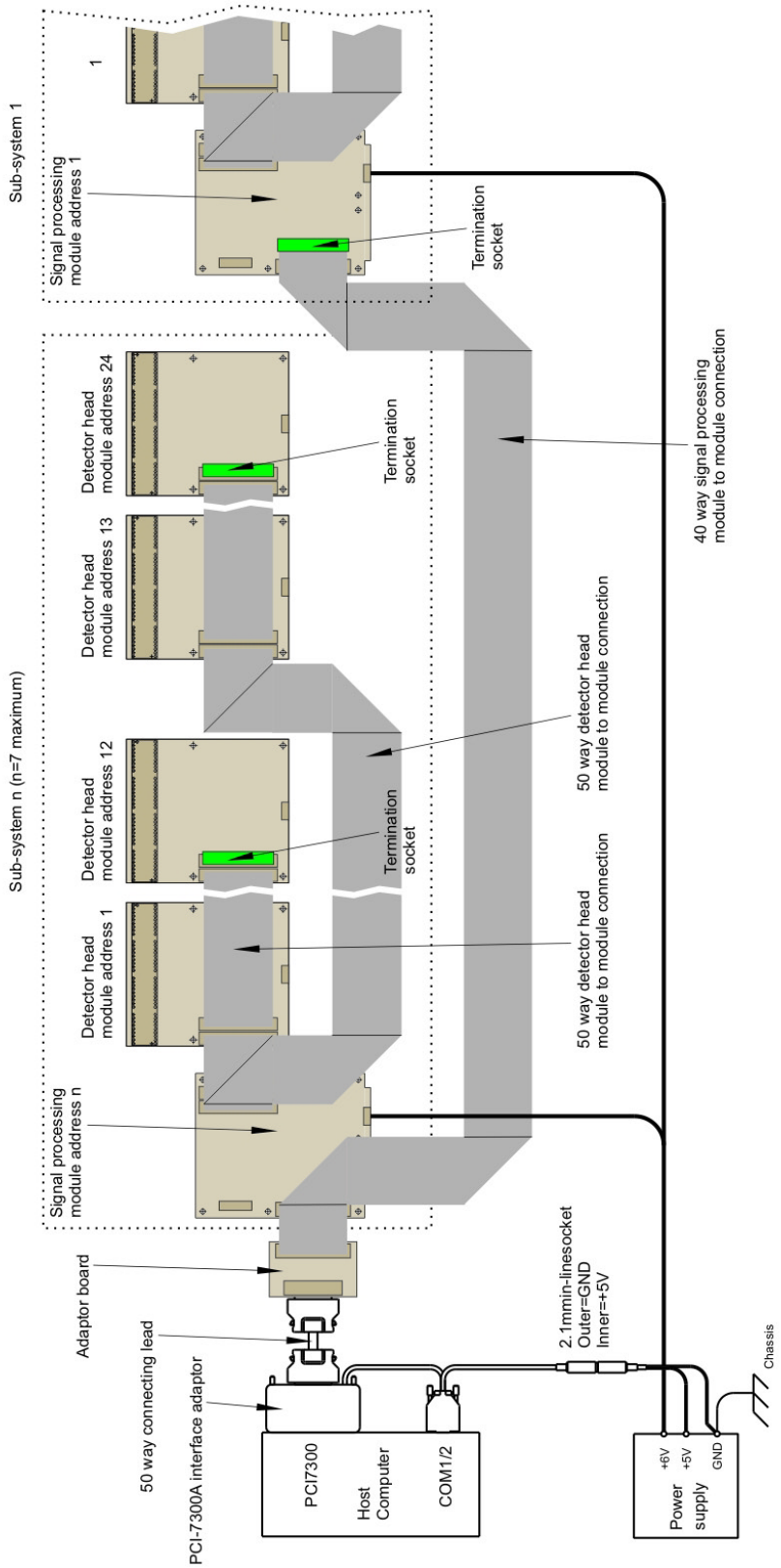
system block diagram for a system of n boards



appendix D

cable interconnections

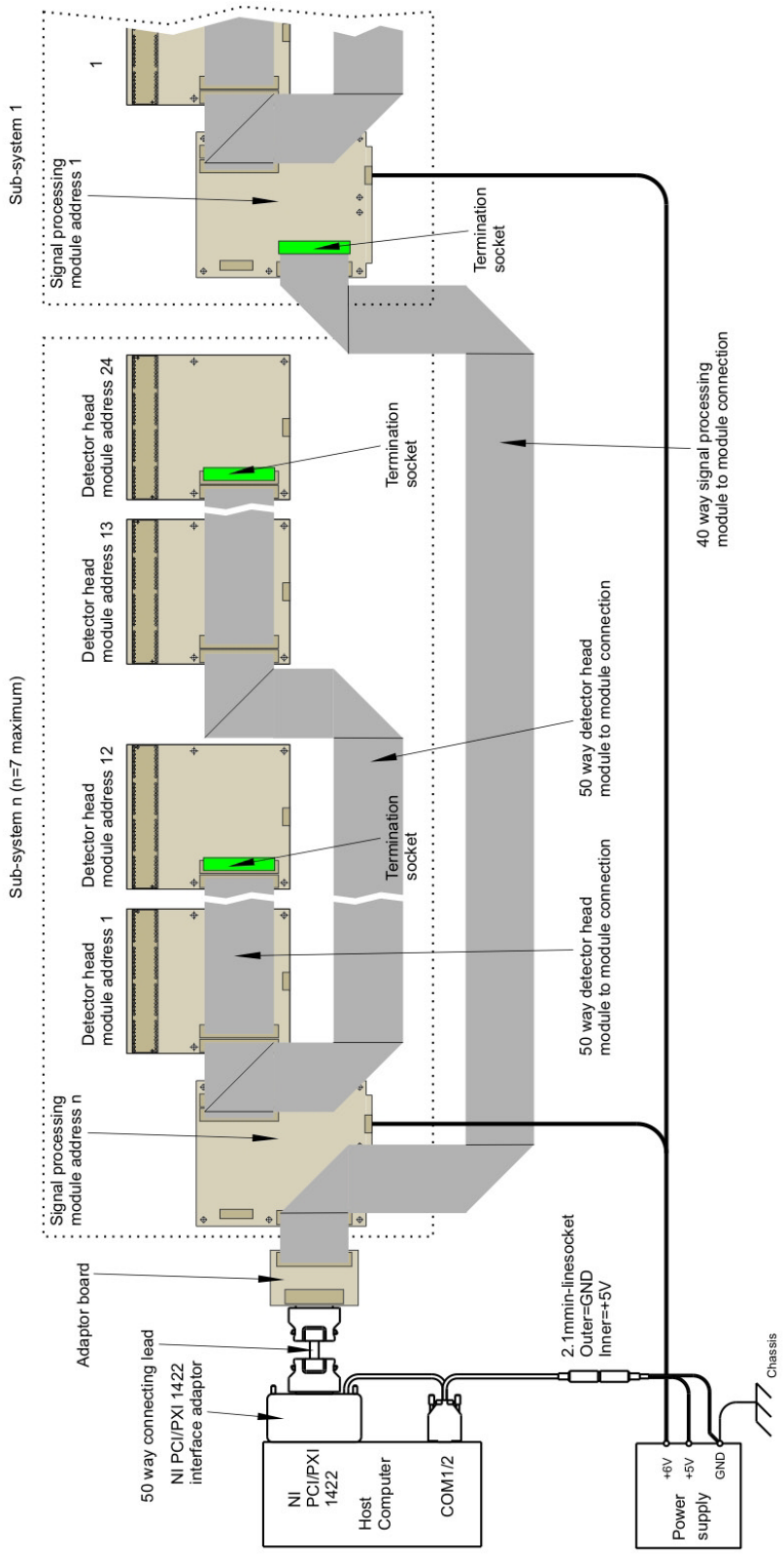
High speed data I/O PCI-7300A connections



System readout direction is fully programmable using switch B and switch C on the signal processing boards, regardless of the module interconnection. Please refer to section 5.2 of this manual.

appendix D (continued)

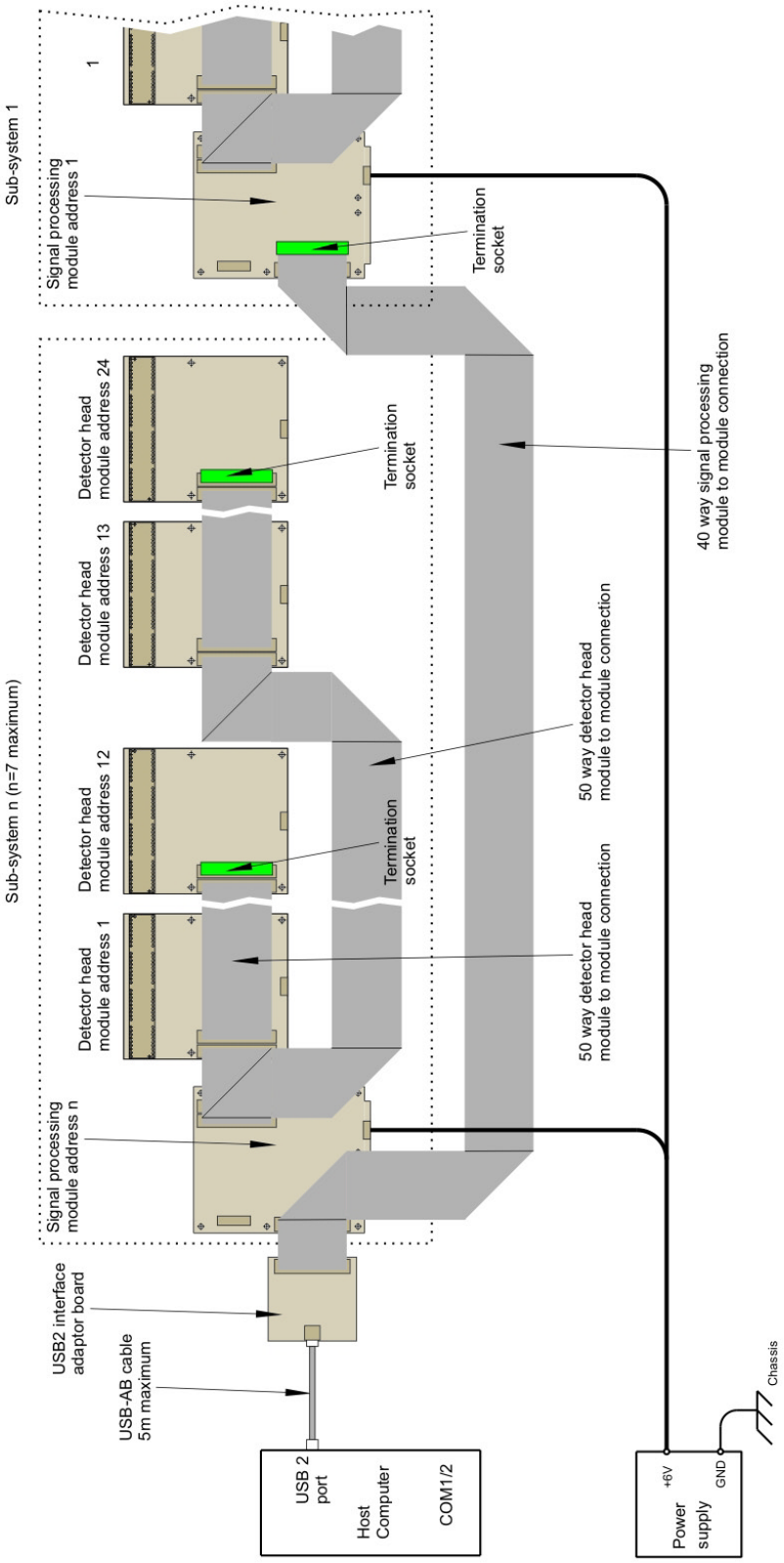
Frame Grabber connections



System readout direction is fully programmable using ble using switch B and switch C on the signal processing ing boards, regardless of the module interconnection. ction. Please refer to section 5.2 of this manual.

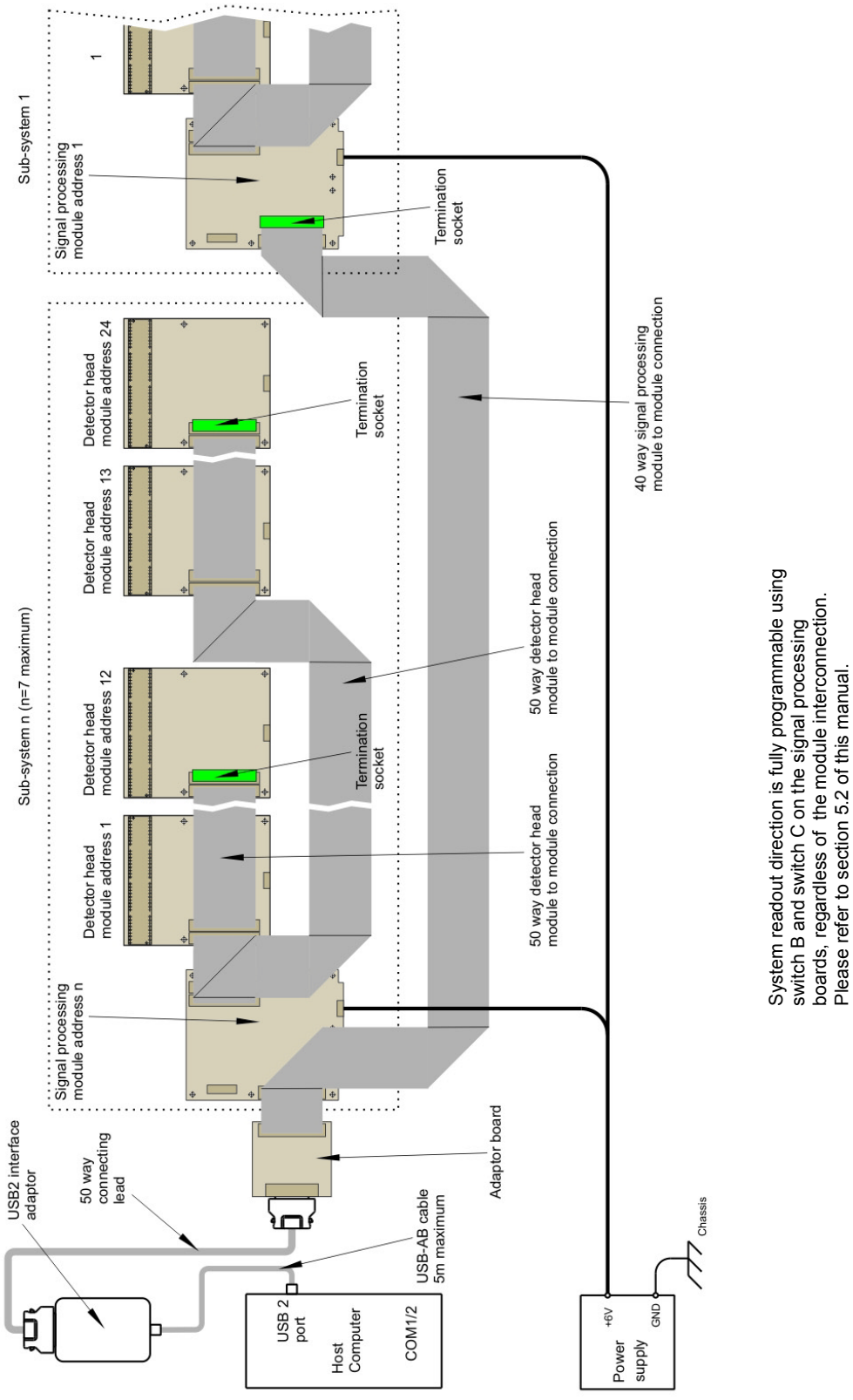
appendix D (continued)

USB2 local connections



appendix D (continued)

USB2 remote connections



appendix E

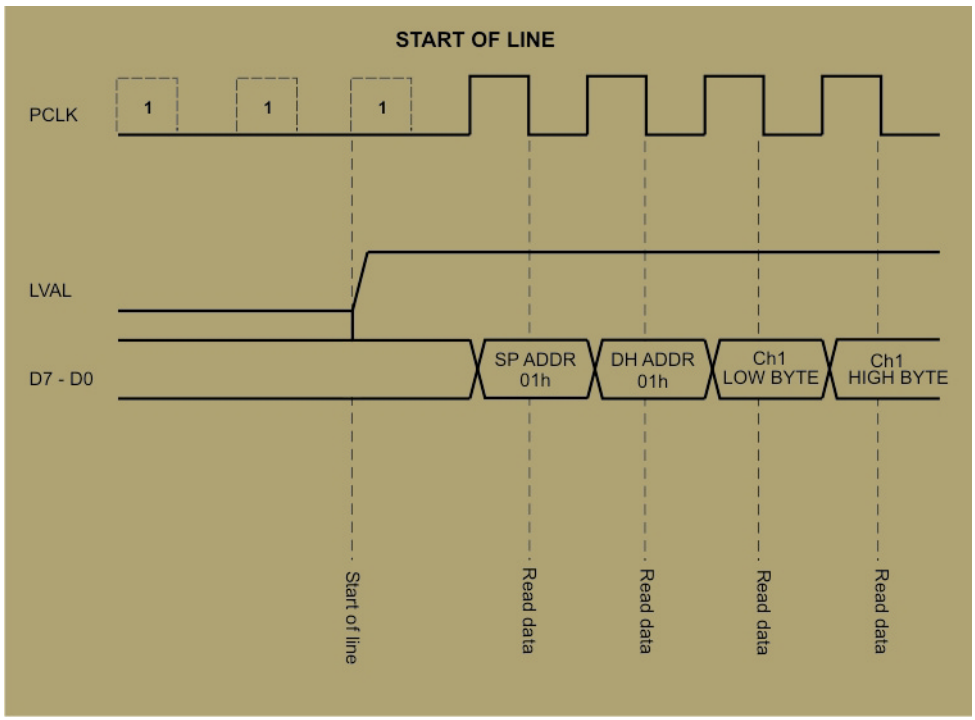
USB2 protocol

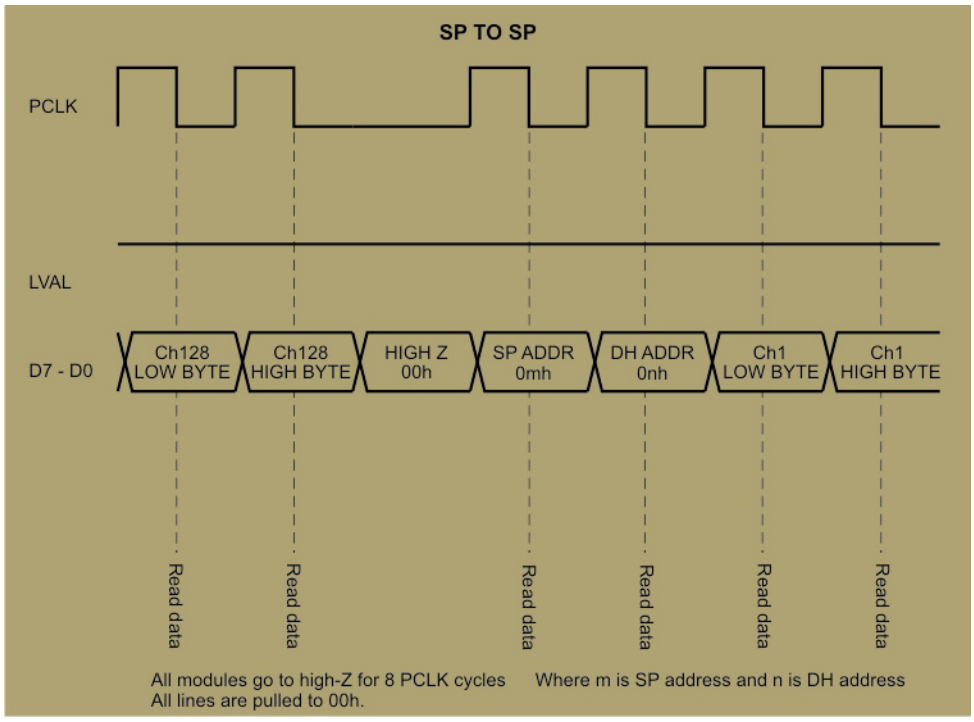
USB2.0 High Speed Mode
Bulk transfer protocol for data acquisition
Integrated control and data interface
XDAS SDK library files available with example code

appendix F

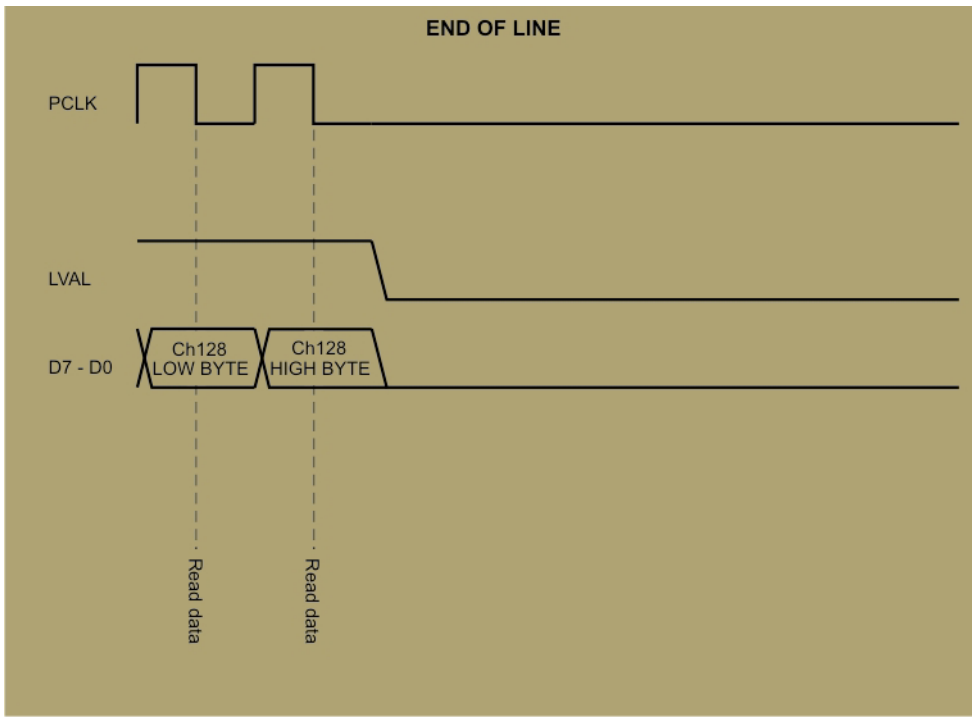
system (data) bus waveforms

These clock pulses are not present if PCLK is gated with LVAL. The un-gated PCLK mode is only available in a single SP board system. Two header bytes are transmitted only if enabled using DIP switch H. The first byte is the SP board ID and the second byte is the DH board ID.



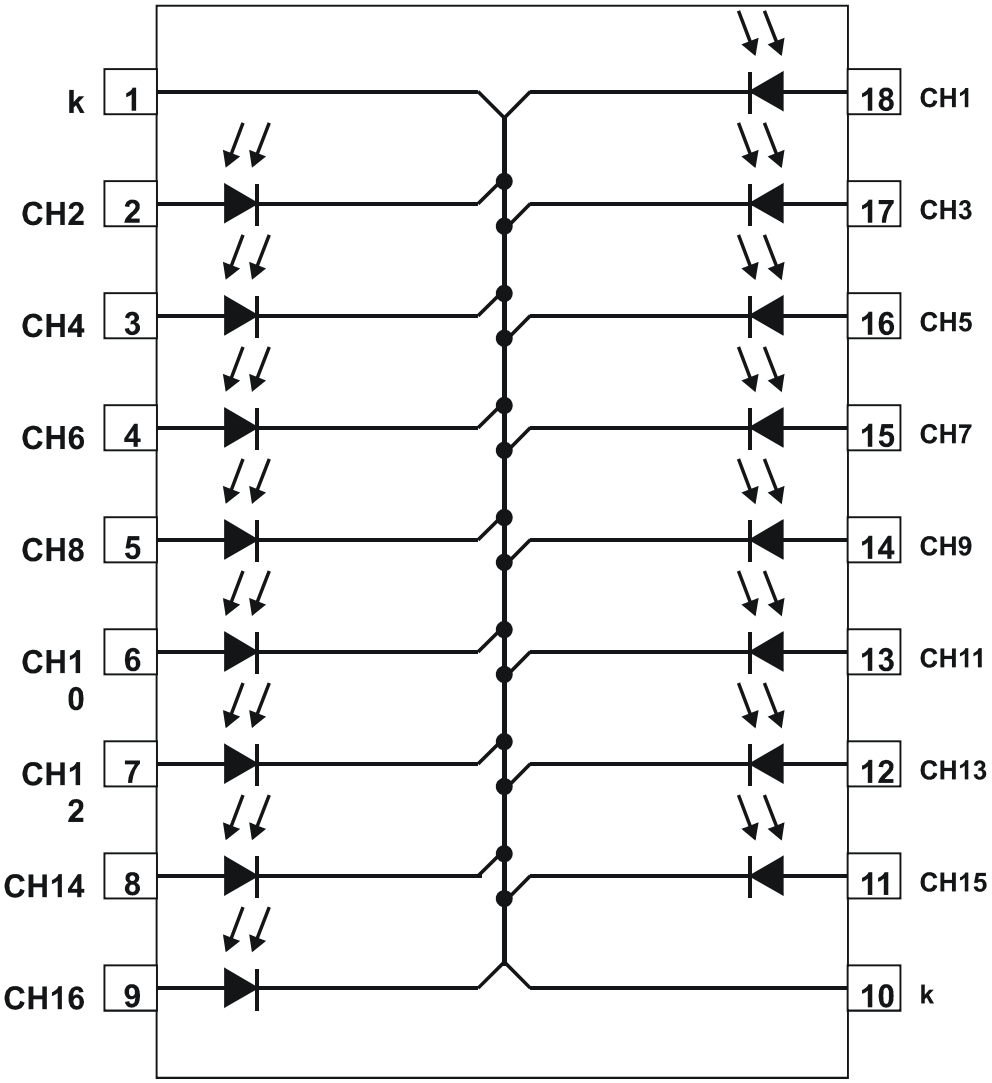


appendix F (continued)



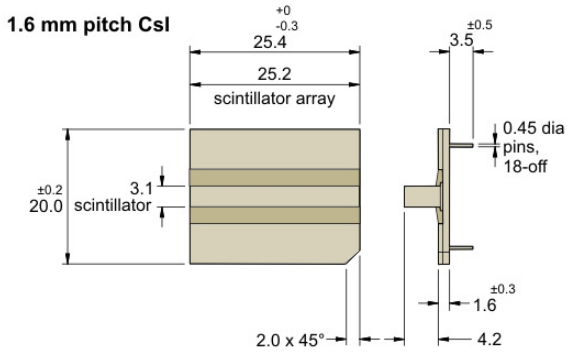
appendix G

16 channel detector pin out

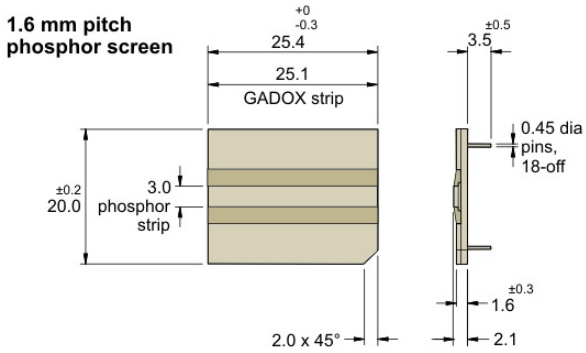


appendix G (continued)

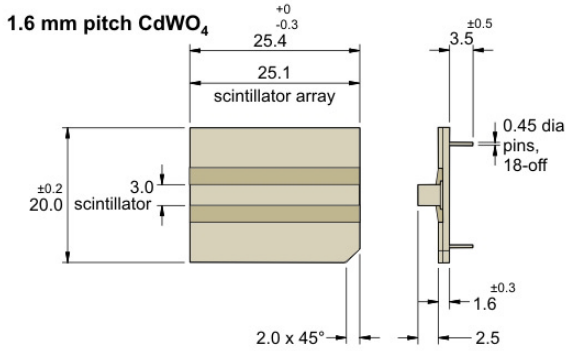
1.6 mm pitch CsI



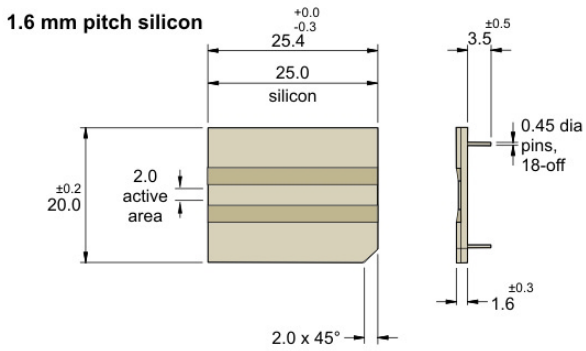
1.6 mm pitch phosphor screen



1.6 mm pitch $CdWO_4$

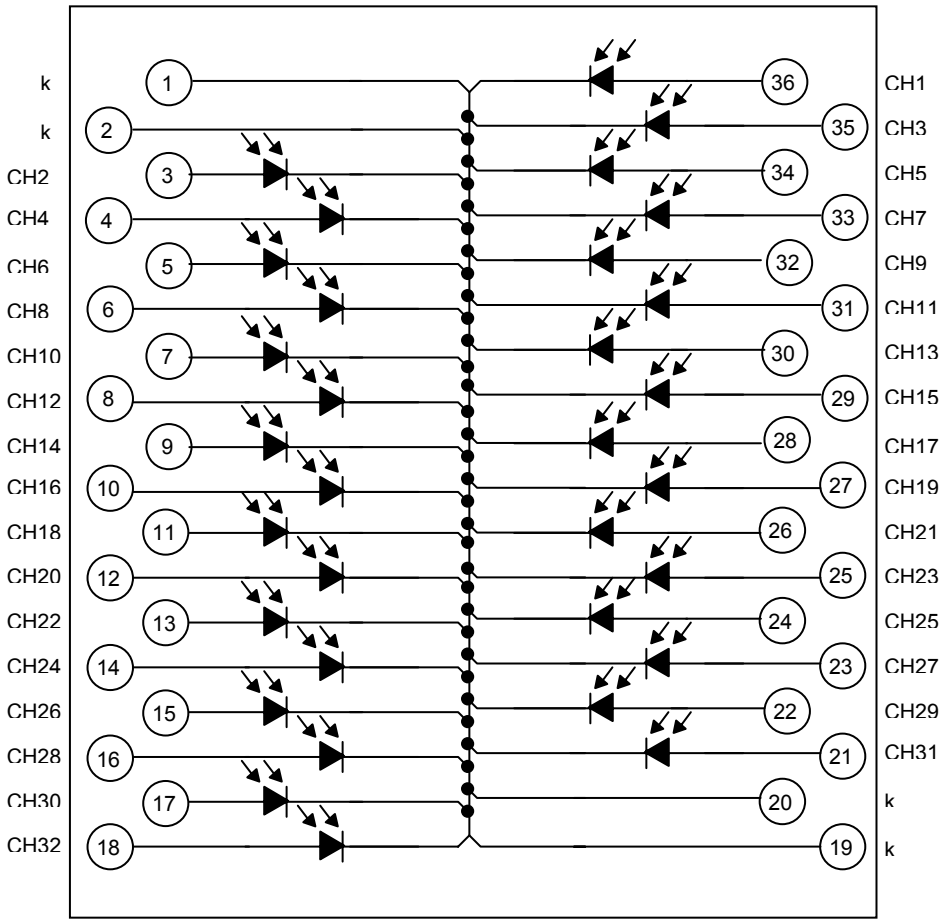


1.6 mm pitch silicon

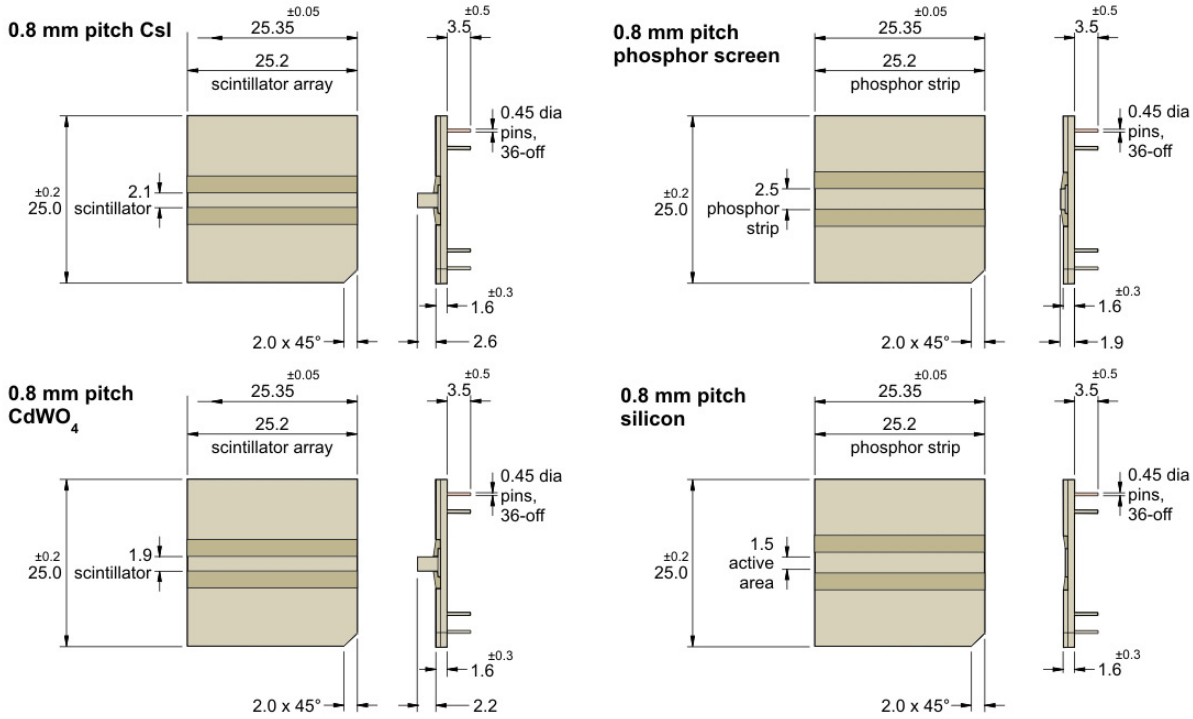


appendix G (continued)

32 channel detector pin out



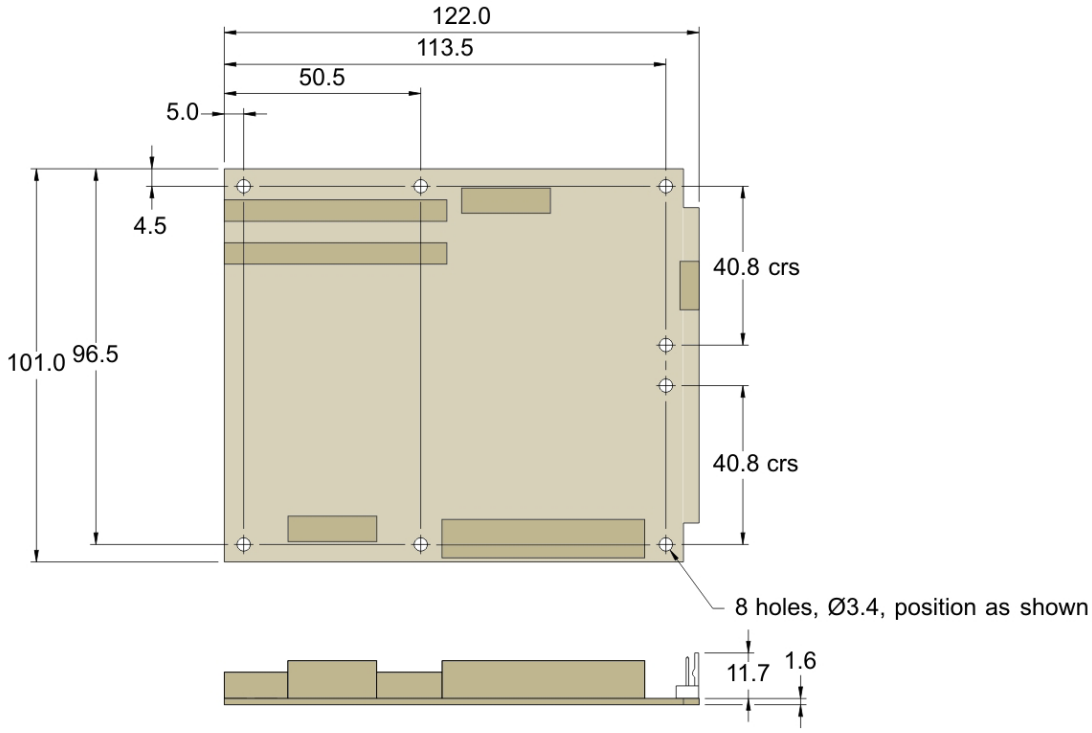
appendix G (continued)



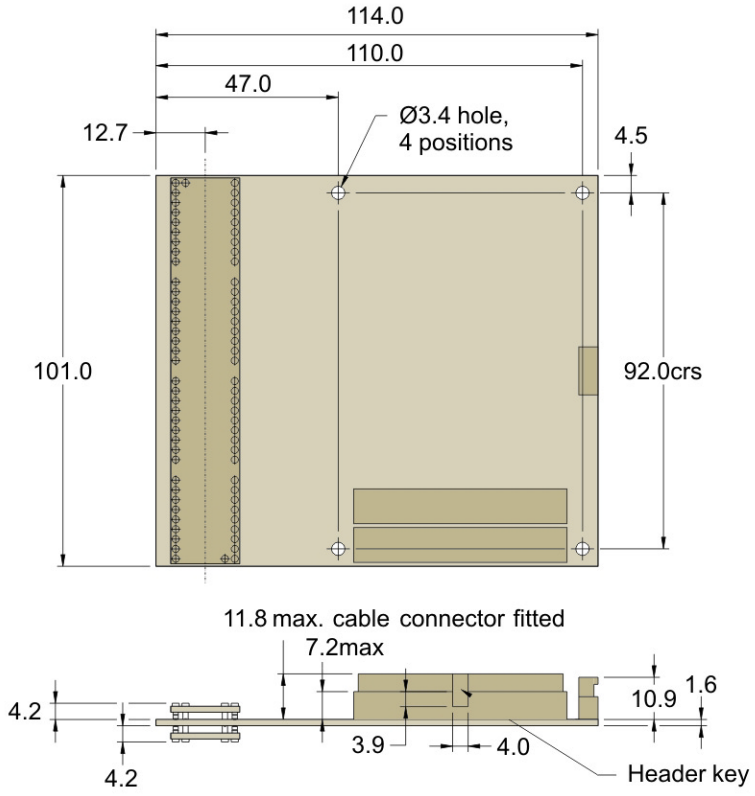
appendix H

outline drawings (in mm)

XDAS-SP2-01 signal processing board



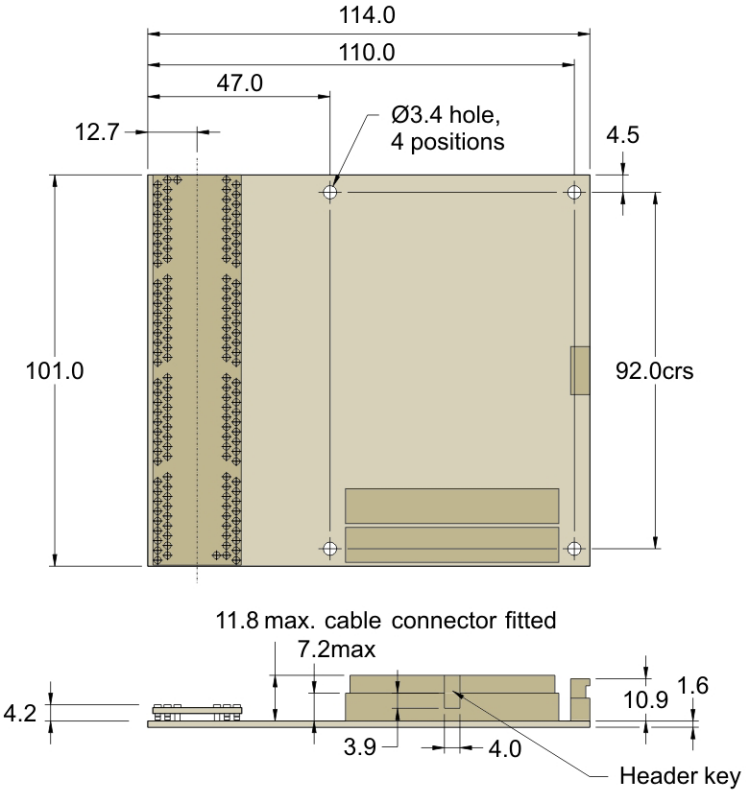
XDAS-DH2-01 1.6mm pitch dual energy detector head



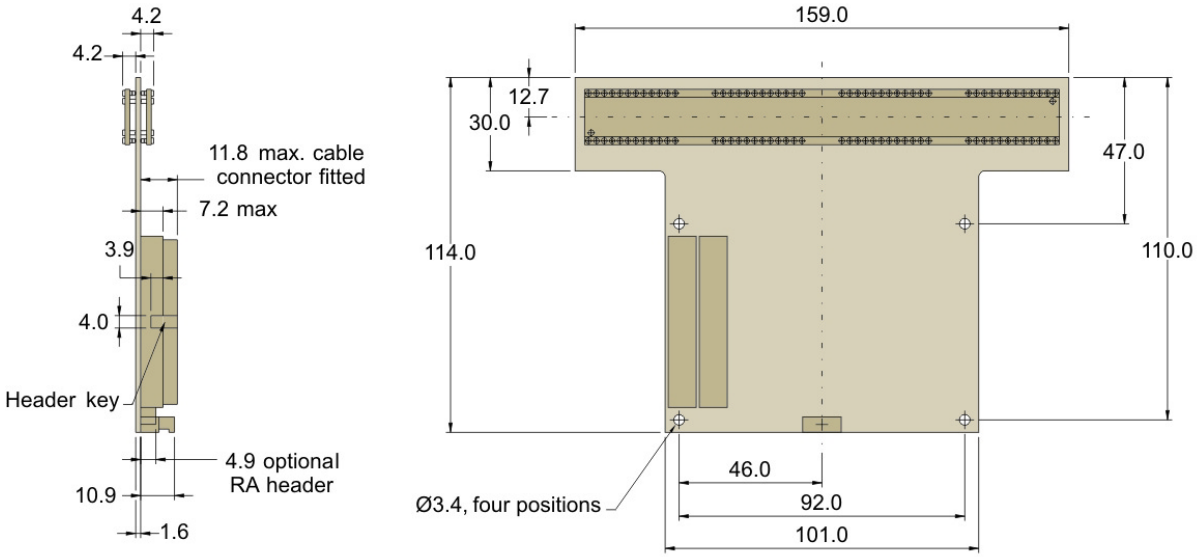
*** To obtain height of detector above board, add detector socket height to detector height (exc. pins)**

appendix H (continued)

XDAS-DH2-10 1.6mm pitch single energy detector head
XDAS-DH2-20 0.8mm pitch single energy detector head



XDAS-DH2-40 2.5mm pitch dual energy detector head



appendix I

peripheral connections

50 way SCSI interface adapters XDAS-DATA3, XDAS-DATA4 or XDAS-DATA6

Pin	Designation	Description	Signal Type
1	RES	Reserved for system use	-
2	VBUS	5V bus supply	DC
3	PCLK+	Pixel clock	RS485
4	VBUS	5V bus supply	DC
5	LVAL+	Line valid	RS485
6	NC	No connection	-
7	RES	Reserved for system use	-
8	NC	No connection	-
9	D0+	Data bit 0	RS485
10	NC	No connection	
11	D1+	Data bit 1	RS485
12	NC	No connection	-
13	D2+	Data bit 2	RS485
14	NC	No connection	-
15	D3+	Data bit 3	RS485
16	DC	No connection	-
17	D4+	Data bit 4	RS485
18	NC	No connection	-
19	D5+	Data bit 5	RS485
20	NC	No connection	-
21	D6+	Data bit 6	RS485
22	GND	Ground	DC
23	D7+	Data bit 7	RS485
24	GND	Ground	DC
25	SCTRL+	Serial control	RS485
26	RES	Reserved for system use	-
27	VBUS	5V bus supply	DC
28	PCLK-	Pixel clock	RS485
29	VBUS	5V bus supply	DC
30	LVAL-	Line valid	RS485
31	NC	No connection	-
32	RES	Reserved for system use	-
33	NC	Not connected	-
34	D0-	Data bit 0	RS485
35	NC	Not connected	-
36	D1-	Data bit 1	RS485
37	NC	Not connected	-
38	D2-	Data bit 2	RS485
39	NC	No connection	-
40	D3-	Data bit 3	RS485
41	NC	No connection	-
42	D4-	Data bit 4	RS485
43	NC	No connection	-
44	D5-	Data bit 5	RS485
45	NC	No connection	-
46	D6-	Data bit 6	RS485
47	GND	Ground	DC
48	D7-	Data bit 7	RS485
49	GND	Ground	DC
50	SCTRL-	Serial control	RS485

appendix I (continued)

USB2 module (Part No. XDAS-USB2)

XDAS interface

Local USB2 adapter connects directly to the system control and data bus using a 40way 2.54mm pitch IDC connector.

Remote USB2 adapter connects to the 50way SCSI cable using the SCSI interface adapters XDAS-DATA3, XDAS-DATA4 or XDAS-DATA6.

Host Interface:

Standard USB B type connector
USB2.0 High Speed Mode
Bulk transfer protocol for data acquisition
Integrated control and data interface
XDAS SDK library files available with example code

appendix I (continued)

PCI7300 Interface Adaptor (Part No. XDAS-485A-TTL)

PCI7300A port (CN1)

Pin	Designation	Description	Signal Type
1 to 50	GND	Ground	-
51 to 82	NC	Not connected	-
83	PCLK	Pixel clock	TTL
84 to 88	GND	Ground	-
80 to 90	NC	Not connected	-
91	FVL	Frame valid	TTL
92	LVAL	Line valid	TTL
93	D7	Data bit 7	TTL
94	D6	Data bit 6	TTL
95	D5	Data bit 5	TTL
96	D4	Data bit 4	TTL
97	D3	Data bit 3	TTL
98	D2	Data bit 2	TTL
99	D1	Data bit 1	TTL
100	D0	Data bit 0	TTL

Serial Port (COM1 or 2)

Pin	Designation	Description	Signal Type
1	NC	Not connected	-
2	NC	Not connected	-
3	TXD	Transmit data	RS232
5	GND	Ground	-
9	NC	Not connected	-

The following pins are connected together

Pin	Designation	Description	Signal Type
4 and 6	DTR and DSR	Data terminal ready and Data set ready	RS232
7 and 8	RTS and CTS	Request to send and Clear to send	RS232

